UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,445	01/23/2002	David J. Potts	TI-27832	6368

23494 7590 12/31/2003

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
GEYER, SCOTT B	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,445	POTTS, DAVID J.	
	Examiner	Art Unit	
	Scott B. Geyer	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *31-38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 22-28* is/are rejected.

7)☒ Claim(s) *12-21,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *0102* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 1-30 in Paper No. 0902 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(e), to provisional application 60/344,161.

Information Disclosure Statement

The reference cited on the IDS, received on 01/23/02, has been considered.

Drawings

The drawings submitted on 01/23/02 by the applicant are acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11, 22 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Farnworth et al. (5,059,899).

As to ***independent claim 1***, Farnworth et al. teach a method of forming a plurality of integrated circuits on a wafer. Farnworth et al. teach first and second

integrated circuit die (30) formed in a first and second positions on a wafer as shown in figure 3, wherein the first and second integrated circuit dies are separated by scribe lines (32). Each integrated circuit die has at least two devices, e.g. a resistor (44) and a transistor (40). The two devices on each integrated circuit die are connected by a metal layers (i.e. control lines) (42). Further, the metal layers (i.e. test circuitry) 46 extend into the scribe line areas and connect to both the devices on the first and second integrated circuit dies.

As to ***claims 2 and 3***, Farnworth et al. teach physically separating/cutting the two dies (column 3, lines 37-40).

As to ***claims 4 and 5***, Farnworth et al. teach severing the metal layer portion which connects the first and second integrated circuit dies (column 4, lines 25 et seq.).

As to ***claim 6***, Farnworth et al. teach forming a contact (46) in electrical communication with the metal layers (i.e., conductive lines) which connect the first and second integrated circuit dies.

As to ***claim 7***, Farnworth et al. teach testing the at least two integrated circuit dies simultaneously (column 3, lines 1-10).

As to ***claim 8***, Farnworth et al. teach forming an electrical contact (i.e., test circuitry) (46) in the scribe area (32).

As to ***claim 9***, Farnworth et al. teach forming an electrical contact (test bonding pad) 34 in the "first area", i.e. within the area defined by the first integrated circuit.

As to ***claim 10***, Farnworth et al. teach forming an electrical contact in the scribe area (36) for testing both of the integrated circuit dies simultaneously, and forming an

electrical contact in both the region of the first IC die and the second IC die. These two electrical contacts are shown in figure 3 by numeral 34. Both of these electrical contacts are communicable with their respective IC circuitry after the dicing step has been performed.

As to ***claim 11***, Farnworth et al. teach the electrical contact (36) in the scribe area as having a larger surface area than the electrical contacts (34) located within the IC die regions.

As to ***claim 22***, Farnworth et al. teach forming a plurality of IC die on the wafer, which comprise a first and second die, as shown by figure 3. Further, Farnworth et al. teach completing circuitry on each of the IC dies and forming a metal layer (i.e., conductive lines) that comprise intra-die portions (i.e., portions within the IC die) and inter-die portions (i.e., portions outside the region defined by the IC die), as is clearly shown by figure 3.

As to ***independent claim 24***, Farnworth et al. teach forming a plurality of IC die on the wafer, which comprise a first and second die separated by scribe lines as shown by figure 3. Farnworth et al. also teach. Further, Farnworth et al. teach completing circuitry on each of the IC dies and forming a metal layer (i.e., conductive lines) that comprise intra-die portions (i.e., portions within the IC die) and inter-die portions (i.e., portions outside the region defined by the IC die), as is clearly shown by figure 3.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al. (5,059,899) in view of Hsu (5,780,161).

As to ***claim 23***, Farnworth et al. teach fabrication of integrated circuits with conductive connectors. Farnworth et al. do not teach formation of the conductive metal connectors using a reticle (i.e., a photomask). However, the use of photomasks is notoriously well known in the art of semiconductor manufacturing. For example, Hsu teach utilizing a reticle to form the metal patterns on an integrated circuit (column 1, line 14 et seq.). At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the invention of Farnworth et al. by using a photomask (i.e., reticle) as taught for example by Hsu, so as to print fine-line width metal features on a small area surface such as a semiconductor substrate, wherein the use of a reticle would enable more features to be formed on a smaller device area substrate.

Claims 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al. (5,059,899) in Farnworth et al. (5,898,186).

As to ***claim 25***, Farnworth et al. ('899) do not teach a plurality of shared contacts in the scribe area wherein each of the plurality of shared contacts is electrically connected to an inter-die portion of at least two of the plurality of integrated circuit die. However, Farnworth et al. ('186) do teach a plurality of shared contacts (fig. 2A numerals 26,28,30) in the scribe area wherein each of the plurality of shared contacts is

electrically connected to an inter-die portion of at least two of the plurality of integrated circuit die (represented by numerals 18A, 18B, 18C, 20A, 20B, 20C). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the method of Farnworth et al. with a plurality of shared contacts as taught by Farnworth et al. so as to maximize efficiency of die testing.

As to ***claim 26***, Farnworth et al. ('186) teach testing multiple die (i.e., simultaneous testing) (see column 9, lines 48 et seq.).

As to ***claim 27***, Farnworth et al. ('899) do not teach a plurality of shared contacts in the scribe area wherein each of the plurality of shared contacts is electrically connected to an inter-die portion of all of the plurality of integrated circuit die in a respective area. However, Farnworth et al. ('186) do teach a plurality of shared contacts (fig. 2A numerals 26,28,30) in the scribe area wherein each of the plurality of shared contacts is electrically connected to an inter-die portion of at least two of the plurality of integrated circuit die (represented by numerals 18A, 18B, 18C, 20A, 20B, 20C). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the method of Farnworth et al. with a plurality of shared contacts as taught by Farnworth et al. so as to maximize efficiency of die testing.

As to ***claim 28***, Farnworth et al. ('186) teach testing multiple die (i.e., simultaneous testing) (see column 9, lines 48 et seq.).

Allowable Subject Matter

Claims 12, 13, 17 and 29 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims (*the applicant is reminded that the entire contents of the claim must be incorporated into the independent claim.*)

The prior art of record and to the examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding:

the limitation of claim 12, wherein a distance D_{max} defined between a plane along the semiconductor substrate and a plane of an intra-die metal connecting layer, and wherein the first metal layer is a distance from the semiconductor substrate equal to or less than D_{max};

the limitation of claim 13, wherein a plurality of isolated metal portions in the first area are electrically isolated from each other;

the limitation of claim 17, wherein a second metal portion is formed in the first area and a third metal portion is formed in the second area, and wherein the second and third metal; portions are electrically disconnected from each other;

the limitation of claim 29, wherein a plurality of shared contacts are formed in a scribe area, wherein each of the plurality of shared contacts is electrically connected to an inter-die portion of at least two of the IC die, and forming at least one isolated contact for each of the plurality of IC die, wherein the isolated contact is electrically isolated from all other of the plurality of IC die (i.e., the isolated contact is electrically isolated from any of the test circuitry and any component that the test circuitry is connected to.)

Claims 14-16 are dependent upon claim 13, claims 18-21 are dependent upon claim 17 and claim 30 is dependent upon claim 29.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer whose telephone number is (703) 306-5866 (***after 1-14-04, the examiner may be reached at 571-272-1958***). The examiner can normally be reached on weekdays, between 10:00am - 6:30pm. E-mail: scott.geyer@uspto.gov

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703) 308-1233. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SBG
December 23, 2003